1. In a data processing system having a system bus and having a processor with a level one cache memory responsively coupled to a level two cache memory which is responsively coupled to a level three cache memory and having a circuit for SNOOPing said system bus , the improvement comprising:

a. First logic which invalidates a corresponding level one cache memory location in response to either a non-local memory write or write ownership request.

2. A data processing system according to claim 1 further comprising second logic which inhibits said first logic from invalidating for mode 3 requests without ownership.

3. A data processing system according to claim 1 further comprising:

a. Third logic which invalidates said corresponding cache memory location in response to a SNOOP hit.

4. A data processing system according to claim 3 further comprising:

a. Fourth logic which retrieves and records data in response to a level one cache memory read miss and a level two cache memory read miss.

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5. A data processing system according to claim 1 further comprising:

a. Fifth logic which determines when said level two cache memory generates a parity error and which in response invalidates said corresponding level one cache memory location.

6. A data processing system comprising:

a. A processor having a level one cache memory;

b. A level two cache memory responsively coupled to said level one cache memory;

c. A level three memory responsively coupled to said level two cache memory; and

d. A first circuit which invalidates a corresponding portion of said level one cache memory in response to a level one cache memory write hit and a level two cache memory write.

7. A data processing system according to claim 6 further comprising:

a. A second circuit which inhibits said first circuit from said invalidating in response to a mode 3 lack of ownership.

8. A data processing system according to claim 6 further comprising:

a. A system memory bus;

b. A third circuit which SNOOPs said system memory bus; and

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c. A fourth circuit which invalidates said corresponding portion of said level one cache memory in response to a SNOOP hit.

9. A data processing system according to claim 6 further comprising:

a. A fifth circuit which retrieves and records data in response to a level one cache memory read miss and a level two cache memory read miss.

10. A data processing system according to claim 6 further comprising:

a. A sixth circuit which detects parity errors of said level two cache memory and invalidates said corresponding portion of said level one cache memory in response to said detected parity error.

11. A method of maintaining validity of data within a level one cache memory of a processor responsively coupled to a level two cache memory which is responsively coupled to a system memory bus comprising:

a. Formulating a write memory request;

b. First experiencing a level one cache memory miss in response to said write memory request;

c. Second experiencing a level two cache memory hit in response to said first experiencing step; and

d. Invalidating a portion of said level one cache memory

corresponding to said write memory request in response to said second experiencing step.

12. A method according to claim 11 further comprising:

a. Inhibiting said invalidating step if said write memory request is mode 3 lacking ownership.

13. A method according to claim 11 further comprising:

a. SNOOPing said system memory bus; and

b. Invalidating said portion of said level one cache memory if said SNOOPing step identifies data corresponding to said write memory request.

14. A method according to claim 11 further comprising:

a. Formulating a read memory request;

b. Third experiencing a level one cache memory read miss; and

c. Retrieving and recording data corresponding to said read memory request.

15. A method according to claim 11 further comprising:

a. Determining whether a reference to said level two cache memory has a parity error; and

b. Invalidate said portion of said level one cache memory in response to said determining said parity error.

16. An apparatus comprising:

a. Means for executing program instructions;

b. Means responsively coupled to said executing means for level one caching data;

c. Means responsively coupled to said executing means and said level one caching means for accessing a data element if said executing means requires accessing of said data element and said level one caching means does not contain said data element;

d. Means responsively coupled to said requesting means for level two caching data; and

e. Means responsively coupled to said level one caching means for invalidating said data element if said data element is a write data element located within said level two caching means.

17. An apparatus according to claim 16 further comprising:

a. Means responsively coupled to said invalidating means for inhibiting said invalidating if said data element is mode 3 without ownership.

18. An apparatus according to claim 16 further comprising:

a. Means responsively coupled to said level two caching means for bussing system memory data;

b. Means responsively coupled to said bussing means for SNOOPing said bussing means; and

c. Means responsively coupled to said SNOOPing means for

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invalidating said data element if said SNOOPing means locates a
corresponding data element and said data element is a write data
element.

5   19. An apparatus according to claim 16 further comprising:

a.   Means responsively coupled to said level two caching
means for retrieving and record said data element if said data
element is a read data element and said level two caching means
experiences a miss.

10   20. An apparatus according to claim 16 further comprising:

a. Means responsively coupled to said level two caching means
for detecting a parity error; and

b. Means responsively coupled to said level one caching means
15 and said detecting means for invalidating said data element if said
detecting means detects said parity error.

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